



Docket No. YOR920030175US1

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Patent Application**

Applicant(s): Allen et al.  
Case: YOR920030175US1  
Serial No.: 10/661,041  
Filing Date: September 12, 2003  
Group: 2811  
Examiner: Cuong Q. Nguyen

Title: Techniques for Patterning Features in Semiconductor Devices

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**AFFIDAVIT UNDER 37 C.F.R. §1.131**

We, the undersigned, hereby declare and state as follows:

1. We are the named inventors of the above-referenced U.S. patent application.

2. On or around November, 2000, we prepared the enclosed document (labeled "Exhibit 1") that evidences a reduction to practice of an invention falling within one or more of the claims of the above-referenced application.

3. On page 3 of the document, an image is shown (situated on the left-hand side of page 3) (hereinafter "the image") that illustrates etching through a photoresist layer (top layer), an antireflective material layer (middle layer) and a portion of a substrate layer (lower layer).

4. As is shown in the image, a critical dimension reduction occurred during etching of the antireflective material layer. This is further evidenced by the caption to the image, which indicates a -30 nanometer critical dimension bias.

5. As shown in the image, critical dimension reduction occurred during etching of the antireflective material layer, as etching is shown to have ceased just following passage through the antireflective material layer.

6. All statements made herein of our own knowledge are true, and all statements made on information and belief are believed to be true.

7. We understand that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001, and may jeopardize the validity of the application or any patent issuing therefrom.

Date: \_\_\_\_\_

\_\_\_\_\_  
Scott D. Allen

Date: \_\_\_\_\_

\_\_\_\_\_  
Katherina E. Babich

Date: \_\_\_\_\_

\_\_\_\_\_  
Steven J. Holmes

Date: \_\_\_\_\_

\_\_\_\_\_  
Arpan P. Mahorowala

Date: \_\_\_\_\_

\_\_\_\_\_  
Dirk Pfeiffer

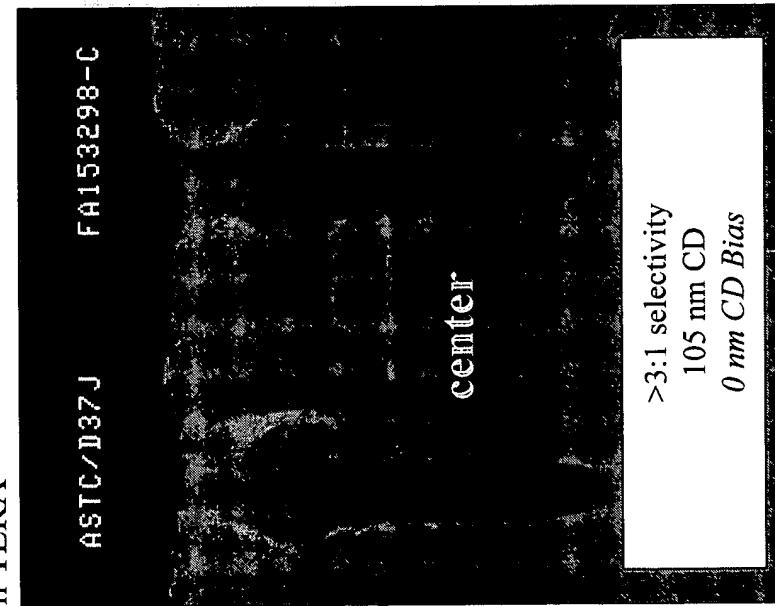
Date: \_\_\_\_\_

\_\_\_\_\_  
Richard Stephan Wise

## DRAM DEVELOPMENT ALLIANCE

PAR-710 Resist  
(350 nm post develop)  
300 nm TERA

TERA Development  
Fluorocarbon Open Etch Processes -  $\text{CHF}_3$  Base



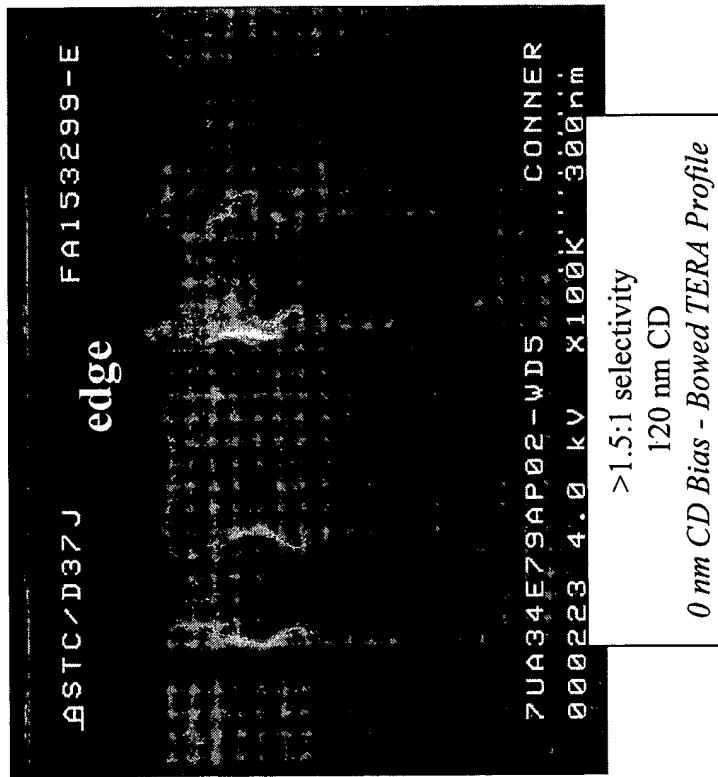
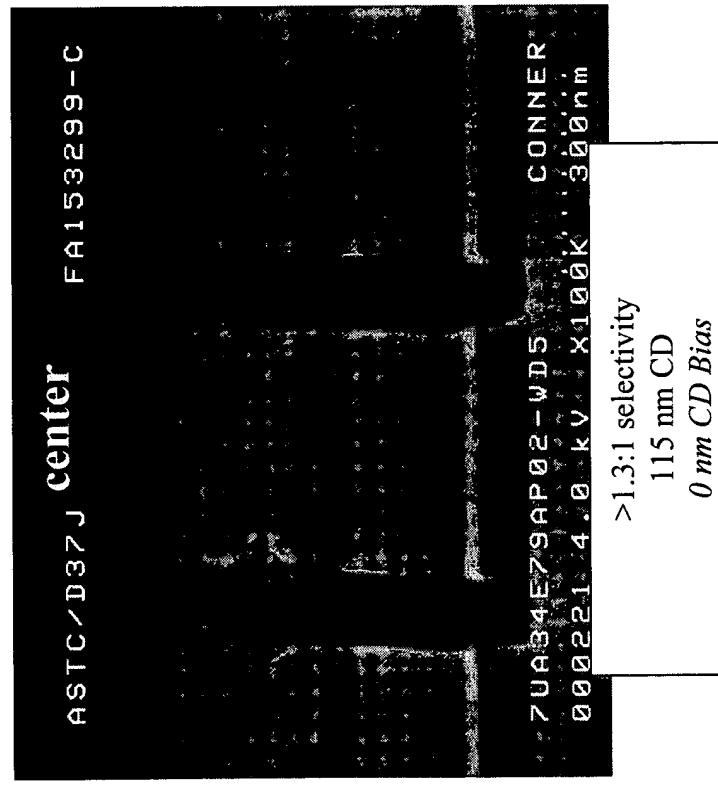
TEL 85 Process:  
 $\text{SiC: 60 secs / 40 mT / 1.4\text{ kW / 5 C}_4\text{F}_8 / 10 \text{CHF}_3 / 100 \text{N}_2 / 5 \text{O}_2 / 150 \text{ Ar}$

- => Increase  $\tau_{\text{RES}}$  results in much improved c/e distribution, lower overall selectivity
- => Too much polymer in center, decrease  $\tau_{\text{RES}}$  to improve profile (CGF system)

# DRAM DEVELOPMENT ALLIANCE

PAR-710 Resist  
(350 nm post develop) Fluorocarbon Open Etch Processes -  $\text{CH}_2\text{F}_2$  Base  
300 nm TERA

## TERA Development



## TEL 85 Process:

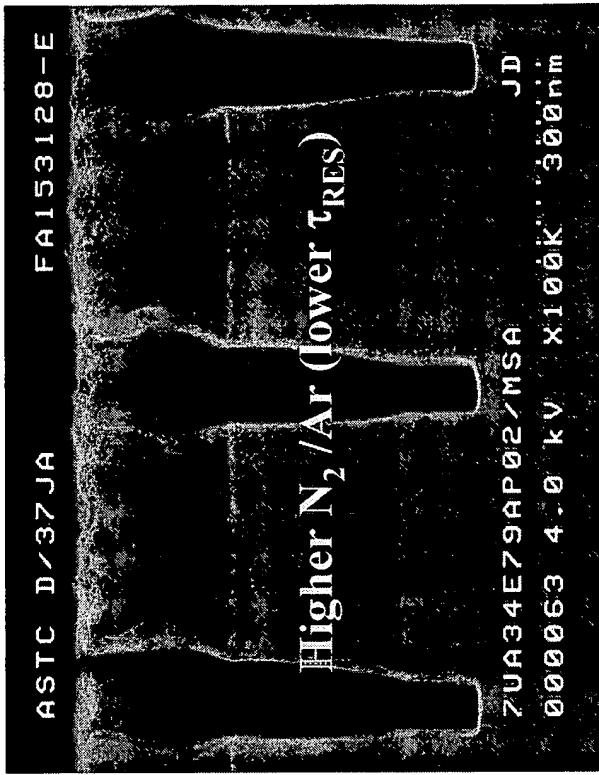
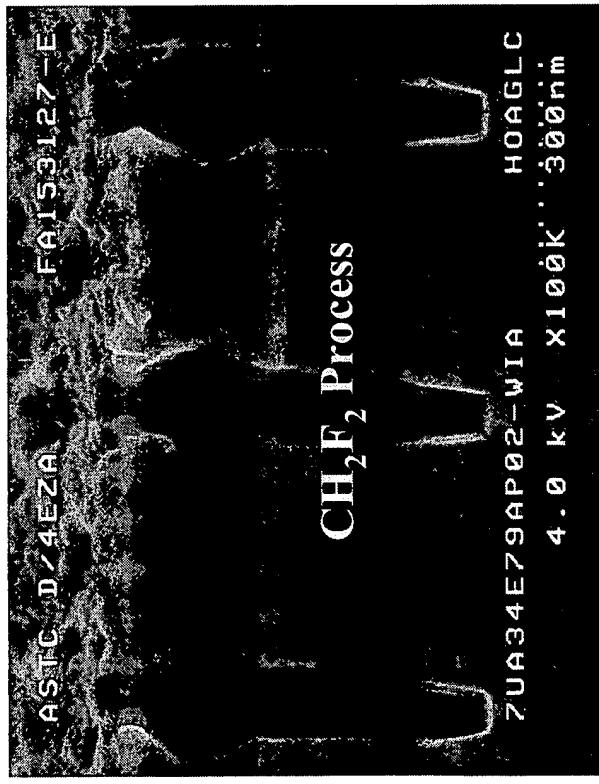
SiC: 60 secs / 40 mT / 1.4kW / 4  $\text{C}_4\text{F}_8$  / 10  $\text{CH}_2\text{F}_2$  / 100  $\text{N}_2$  / 5  $\text{O}_2$  / 200 Ar

=> Addition of 20%  $\text{N}_2$ , reduction 20%  $\text{C}_4\text{F}_8$  to  $\text{CH}_2\text{F}_2$  base chemistry eliminated previous CD bias  
=> Much reduced selectivity (extreme sensitivity to  $\text{C}_4\text{F}_8$  flow)

# DRAM DEVELOPMENT ALLIANCE

PAR-710 Resist  
300 nm TERA

## TERA Development F Open Etch Processes



>2:1 selectivity  
(200 nm PR + 80 nm Polymeric Cap)  
-30 nm CD Bias (c/e similar)

>2:1 selectivity  
(220 nm PR Remains)  
-20 nm c CD Bias, -120 nm e CD Bias

TEL 85 Process:  
SiC: 60 secs / 40 mT / 1.4kW / 5 C<sub>4</sub>F<sub>8</sub> / 10 CH<sub>2</sub>F<sub>2</sub> / 80 N<sub>2</sub> / 5 O<sub>2</sub> / 200 Ar

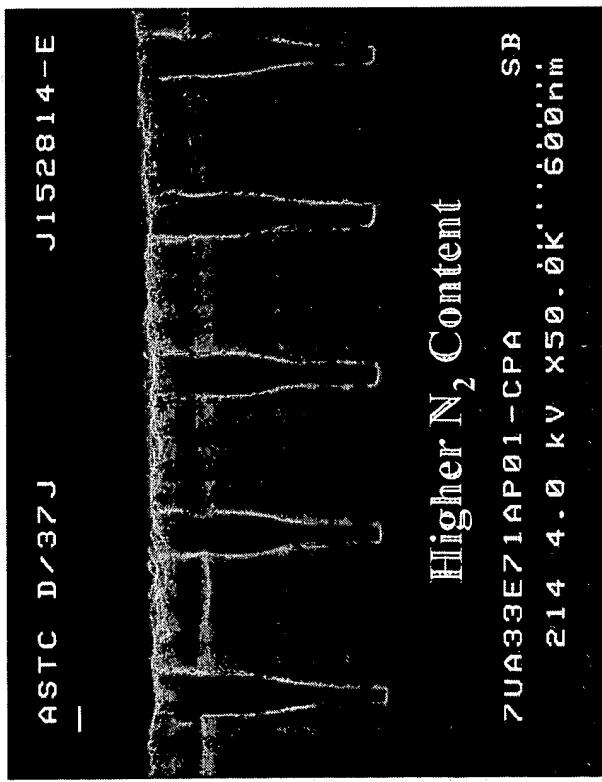
TEL 85 Process:  
SiC: 60 secs / 40 mT / 1.4kW / 5 C<sub>4</sub>F<sub>8</sub> / 10 CHF<sub>3</sub> / 100 N<sub>2</sub> / 5 O<sub>2</sub> / 250 Ar

- => Reduce CH<sub>2</sub>F<sub>2</sub> flow (less polymer)
- => Flatten profile (similar to earlier experiments)
- => Reduce CD Bias
- => Increase t<sub>RES</sub> (Ar/N<sub>2</sub> flow) (based on previous)
- => Flatten profile (similar to earlier experiments)
- => Reduce CD Bias

# DRAM DEVELOPMENT ALLIANCE

PAR-710 Resist  
300 nm TERA

## TERA Development F Open Etch Processes

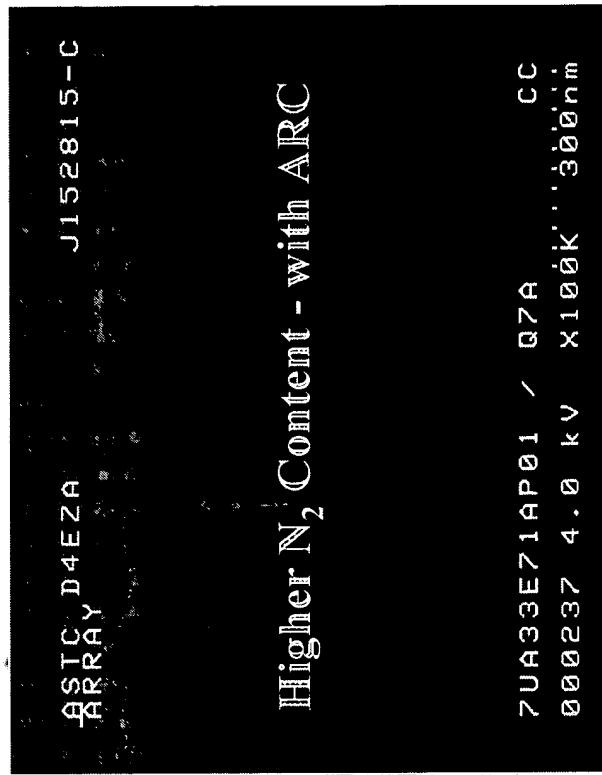


TEL 85 Process:  
SiC: 90 secs / 40 mT / 1.4kW / 5 C<sub>4</sub>F<sub>8</sub> / 10 CHF<sub>3</sub> / 80 N<sub>2</sub> / 5 O<sub>2</sub> / 200 Ar

TEL 85 Process:  
SiC: 90 secs / 150 mT / 500 W / 10 O<sub>2</sub> / 500 Ar / 20 CH<sub>2</sub>F<sub>2</sub>

TEL 85 Process:  
SiC: 90 secs / 40 mT / 1.4kW / 5 C<sub>4</sub>F<sub>8</sub> / 10 CHF<sub>3</sub> / 80 N<sub>2</sub> / 5 O<sub>2</sub> / 200 Ar

- => Continue N<sub>2</sub> increase
- => Tune c/e overetch
- => Flatten profile (similar to earlier experiments)



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